In the Claims:

Claims 1-3 (Cancelled).

4. (Currently Amended) A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device comprising:

a channel coding/decoding stage comprising

an interleaver,

a deinterleaver, ~~and~~

a shared memory having a minimum size based upon a maximum bit rate of the group of predetermined bit rates and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device,

a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N, and

said interleaver providing convolutional interleaving of I branches with i - 1 blocks of M bytes, and said deinterleaver providing convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

Claims 5 and 6 (Cancelled).

7. (Currently Amended) The device according to Claim 4 ~~Claim 6~~ wherein the size of the first memory space is equal to I x (I -1) x M/2 bytes, the size of the second memory space is equal to I' x (I' - 1) x M'/2 bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

8. (Currently Amended) The device according to Claim 4 ~~Claim 6~~ wherein said interleaver and said deinterleaver respectively comprise a first addressing device and a second addressing device, said first and second addressing devices each comprising:

a first counter defining the relative index i or i' of a branch and having a counting limit value;

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value;

a third counter defining the current index of a block in the branch with index i or i' to be incremented each time the block in the branch with index i or i' has M or M' bytes; and

an intermediate calculation device for calculating the address of each branch in said memory from the content of said first counter.

9. (Previously presented) The device according to Claim

8 wherein said first addressing device further comprises a first address determination device for determining successive read and write addresses in said memory of data successively delivered to said interleaver and said first address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, and the parameter M.

10. (Previously presented) The device according to Claim 8 wherein said second addressing device further comprises a second address determination device for determining successive read and write addresses in said memory of data successively delivered to said deinterleaver and said second address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, the parameter M', and the size of the first memory space.

11. (Previously presented) The device according to Claim 4 wherein said memory comprises a random access memory.

12. (Previously presented) The device according to Claim 4 wherein said memory comprises a dual-port memory.

13. (Currently Amended) A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device

comprising:

a channel coding/decoding stage comprising

an interleaver,

a deinterleaver,

a shared random access memory whose minimum size is fixed as a function of a maximum bit rate of the group of predetermined bits and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device, and

a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N.

said interleaver providing convolutional interleaving of I branches with i - 1 blocks of M bytes, and said deinterleaver providing convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches, said interleaver and said deinterleaver respectively comprising a first addressing device and a second addressing device, said first and second addressing devices each comprising

a first counter defining the relative index i or i' of a branch and having a counting

limit value,

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value,

a third counter defining the current index of a block in the branch with index i or i' to be incremented each time the block in the branch with index i or i' has M or M' bytes, and

an intermediate calculation device for calculating the address of each branch in said random access memory from the content of said first counter.

Claim 14 (Cancelled).

15. (Currently Amended) The device according to Claim 13 ~~Claim 14~~ wherein the size of the first memory space is equal to I x (I - 1) x M/2 bytes, the size of the second memory space is equal to I' x (I' - 1) x M'/2 bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

Claims 16 (Cancelled).

17. (Currently Amended) The device according to Claim 13 ~~Claim 16~~ wherein said first addressing device further comprises a first address determination device for determining

successive read and write addresses in said random access memory of data successively delivered to said interleaver and said first address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, and the parameter M.

18. (Currently Amended) The device according to Claim 13 ~~Claim 16~~ wherein said second addressing device further comprises a second address determination device for determining successive read and write addresses in said random access memory of data successively delivered to said deinterleaver and said second address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, the parameter M', and the size of the first memory space.

19. (Previously presented) The device according to Claim 13 wherein said random access memory comprises a dual-port memory.

20. (Currently Amended) A method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising:

interleaving and deinterleaving the digital data;

setting a minimum size of a shared memory based upon a

maximum bit rate of the group of predetermined bit rates; ~~and~~

assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device;

performing Reed-Solomon coding and decoding for a length N of the digital data; and

the interleaving providing convolutional interleaving of I branches with i - 1 blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

Claims 21-22 (Cancelled).

23. (Currently Amended) The method according to Claim 20 ~~Claim 22~~ wherein the size of the first memory space is equal to I x (I - 1) x M/2 bytes, the size of the second memory space is equal to I' x (I' - 1) x M'/2 bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

24. (Previously presented) The method according to Claim 20 wherein the memory comprises a random access memory.